ANALOG DEVICES

AN-260
APPLICATION NOTE

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Using Digitally Programmable Delay Generators

by Allen Hill

The AD9500 and AD9501 digitally programmable delay generators are versatile parts, useful in numerous applications. The parts are designed for use in automatic test equipment as a deskew element for digital data lines. The versatility of the AD9500 and AD9501 for generating programmable delays allows them to be used in applications which range from ATE to communications, computers, disk drives, lasers, and ultrasound systems. This note describes how best to apply these parts in some of these applications.

GENERAL DESCRIPTION

A digitally programmable delay generator delays a digital edge by a programmed amount of time. Figure 1 shows the basic function of a programmable delay generator. The delay through the device is controlled by an N-bit digital word. This is the programmed delay. A trigger pulse is applied to the input, and after a fixed propagation delay, (t_{PD}), the pulse edge appears a program delay later at the output.

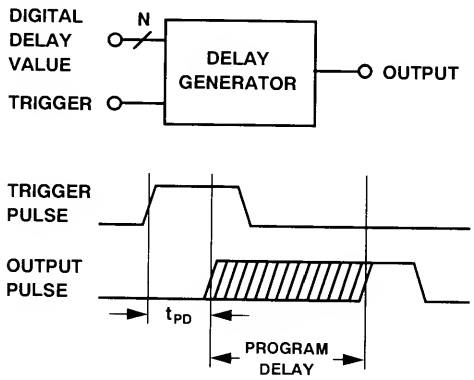


Figure 1. Programmable Delay Generator

The AD9500 (ECL) and AD9501 (TTL) use a ramp/comparator/DAC architecture as shown in Figure 2. One input of a high speed comparator is driven by a digital-to-analog converter (DAC). The DAC is used to set a reference voltage at this comparator input. The other input is connected to a ramp generator. The ramp generator is started by applying a pulse to the trigger input of the delay generator. When the ramp voltage crosses the comparator threshold set by the DAC, the output of the comparator switches.

This output is delayed from the trigger pulse by an amount of time which is proportional to the DAC digital input code and the slope of the ramp. Altering the digital delay value changes the DAC output voltage, which alters the delay through the circuit. The slope of the ramp is controlled with external components.

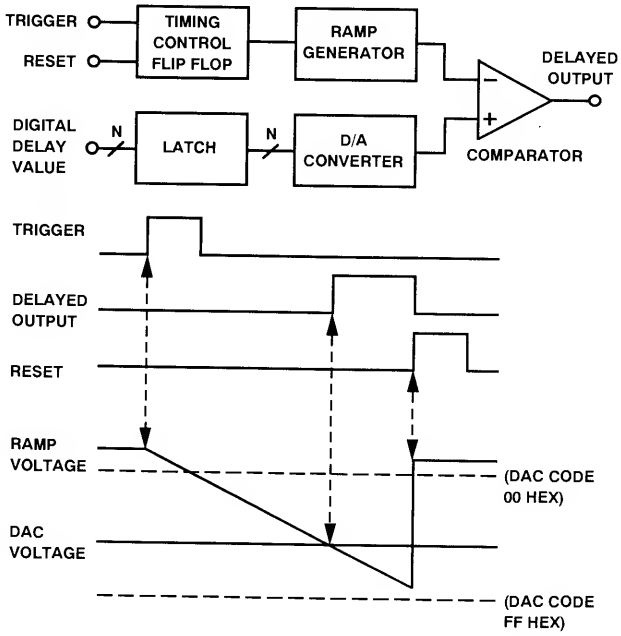


Figure 2. Delay Generator Block Diagram and Basic Timing

Once the comparator has switched, the ramp generator and comparator must be reset so that the device can be triggered again. One method of accomplishing the reset is to connect the output of the delay generator to the reset pin. This results in an output pulse width which is equal to the reset propagation delay of the device (7 ns to 15 ns). An alternate, and versatile method of resetting the device is to use an external signal which meets the timing requirements of the part. An external reset signal allows the pulse width to be controlled and makes system integration of the delay signal easier.

Full-Scale Range Setting

The full-scale range of the generator is the span over which the delay can be programmed. This range is divided into 256 equal delays by the 8-bit digital delay value. The full-scale range of the delay generator is configured by connecting R_{SET} and C_{EXT} as shown in Figure 3. Additional information is available on the AD9500 and AD9501 data sheets. The range can be adjusted from a minimum of 2.5 ns out to 10 μs and beyond.

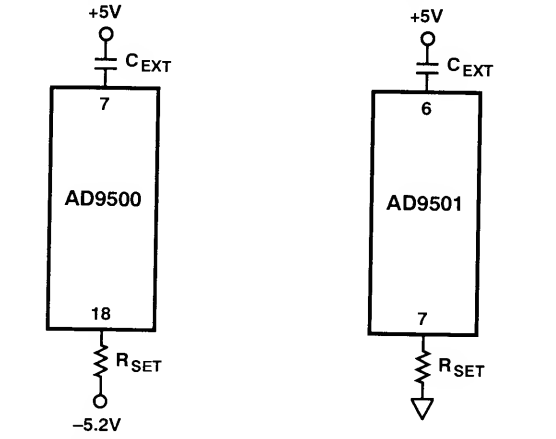


Figure 3. Setting Full-Scale Range on the AD9500 and AD9501

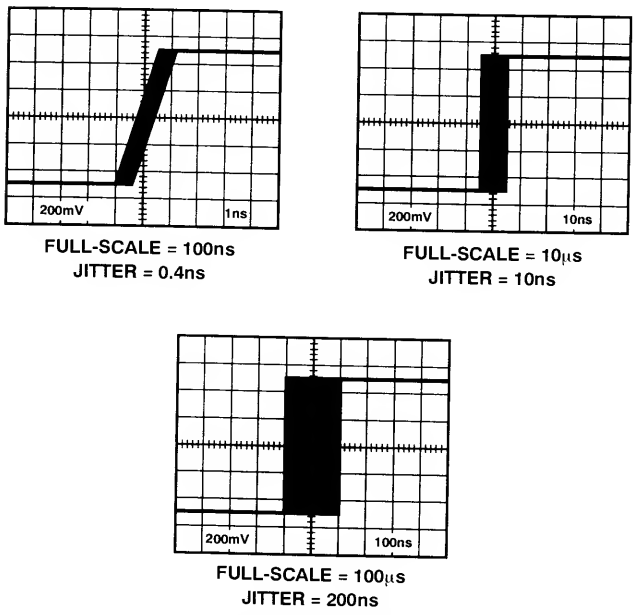


Figure 4. Output Jitter at Various Full-Scale Settings for the AD9500 and AD9501

The maximum full-scale range of these devices depends on the amount of jitter the application can tolerate. Jitter is the variation of delay through the device with subsequent trigger pulses. An increase in full-scale results in an increase in jitter of the output delay. As the full-scale is increased, the slope of the ramp is decreased, resulting in a longer period of time that the ramp is in the comparator transition region. Any noise on the ramp or DAC during this time can cause the comparator to switch. Figure 4 illustrates the output jitter with various full-scale delay settings.

The full-scale range can be adjusted by switching different values of resistance into the R_{SET} pin. A digitally controlled resistor can also be used to provide this function. A programmable full-scale circuit is generated by using a DAC to control the current flow into the R_{SET} pin as shown in Figure 5. The R_{SET} pin of the AD9500 is biased at approximately −4.3 V and requires a current source to set full scale. The bias on the R_{SET} pin of the AD9501 is about 0.5 V and can be used in a similar manner.

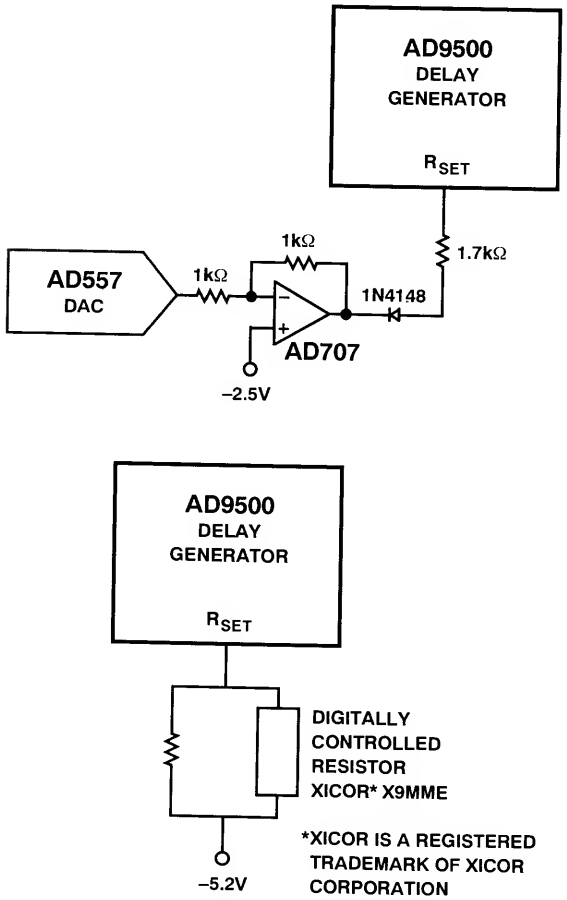


Figure 5. Programmable Full-Scale Range Using a DAC or a Digitally Controlled Resistor

C_{EXT} should not be switched on the AD9500 or AD9501 to provide a programmable full-scale range. The noise pickup on the interconnects can cause false triggering at the input of the device.

When C_{EXT} is increased to extend full-scale range, the reset propagation delay increases because the larger capacitance must be discharged to reset the ramp.

The propagation delay is the time required for the ramp to reach the first DAC threshold. The slope of the ramp is determined by the full-scale setting, which means the propagation delay will change with full-scale range. The propagation delay of the AD9500 and AD9501 can be calculated from the equations shown below.

AD9500 Prop Delay = 5 ns + 0.18 × (Full-Scale Range); Offset Pin Open

AD9501 Prop Delay = 8 ns + 0.18 × (Full-Scale Range); Offset Pin Grounded

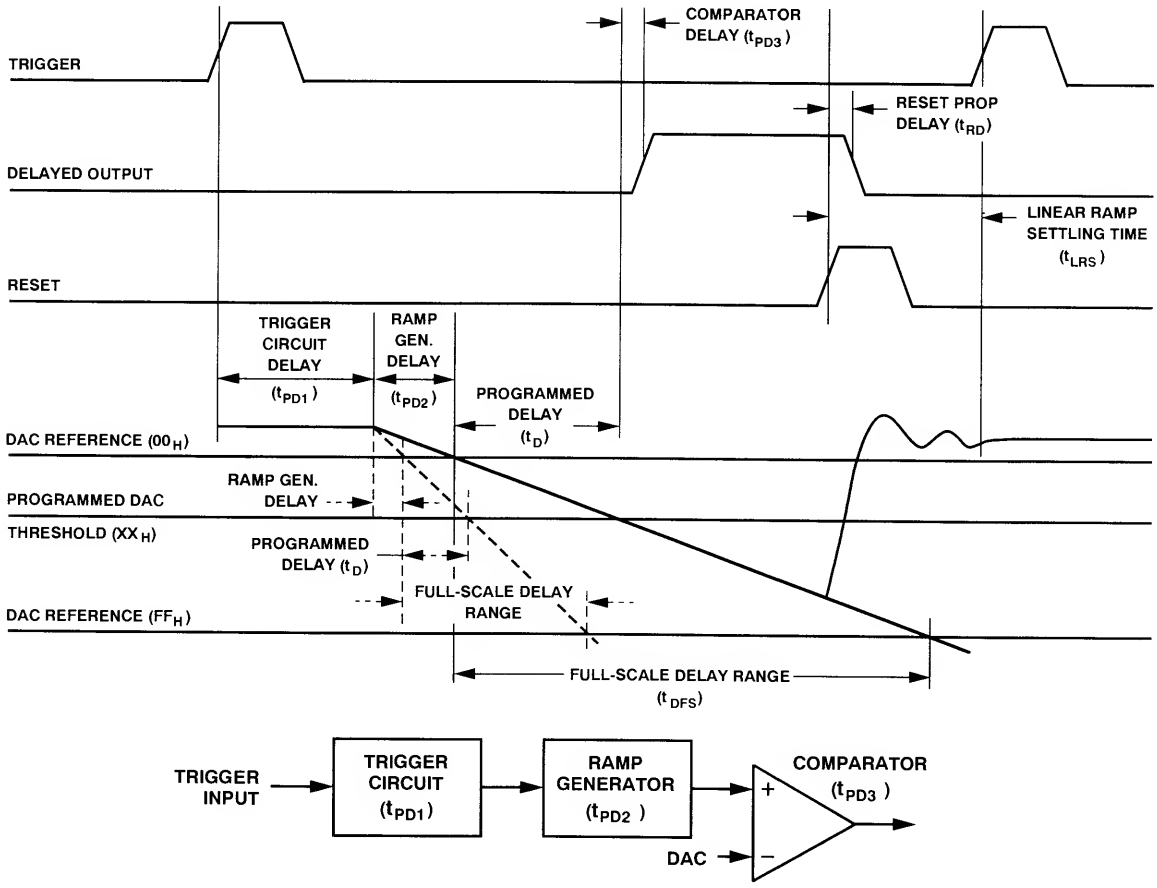
Each device has an offset pin which can be used to adjust the prop delay. This adjustment should only be used to match the prop delays of more than one device in a system. There is not sufficient range to zero the prop delay, and if the offset is adjusted too low, false triggers will occur.

Timing for the AD9500 and AD9501

Figure 6 illustrates the timing requirements of the AD9500 and AD9501. The trigger delay through the generator is made up of four separate parts:

1. Trigger Circuit Delay
2. Ramp Generator Delay
3. Program Delay
4. Comparator Delay

Trigger circuit delay, ramp generator delay, and comparator delay make up the propagation delay of the device. Ramp generator delay is dependent on full-scale range, as discussed earlier. The program delay is the amount of delay programmed by the 8-bit digital value.



MINIMUM PROPAGATION DELAY = (t_{PD}) = (t_{PD1}) + (t_{PD2}) + (t_{PD3})

MAXIMUM PROPAGATION DELAY = MINIMUM PROPAGATION DELAY (t_{PD}) + FULL-SCALE DELAY RANGE (t_{DFS})

TOTAL DELAY = (t_{PD}) + (t_D)

Figure 6. Delay Generator Timing

The reset input also has delays associated with it:

1. Reset Propagation Delay
2. Linear Ramp Settling Time

The reset propagation delay is the time from the edge of the reset signal until the output of the comparator resets. The linear ramp settling time is the time from the edge of the reset signal until the ramp has settled to 8-bit accuracy. The reset delays are not cumulative because they are reset in parallel. This means that the linear ramp settling time determines the reset time when triggering at a random rate because it is the longer of the two delays.

However, if the device is triggered at a constant rate, the reset propagation delay determines the reset time. A constant update rate causes the ramp to settle to the same value, even though this is not the theoretical final value. This means the ramp will always start at the same point.

The trigger delay, combined with the reset delay, determines the maximum rate at which the device can be updated. When the update is constant and the output pulse is used for a reset signal, the following equation can be used to determine the maximum update rate.

Max Update = 1 / [Trigger Delay + Reset Delay + Reset to Trigger Holdoff]

where

Trigger Delay = Prop Delay + Full-Scale Delay

and

Reset Delay = Reset Prop Delay

In applications where the update is not constant, the only change in the above equation will be that the reset delay will be equal to the linear ramp settling time. When the digital code is being changed between trigger pulses, the settling time for the DAC must also be included to determine the maximum update rate.

Considerations When Using the AD9500

The $\overline{QR}$ output of the AD9500 is included to provide a separate output to reset the device. This output does not have the drive capability of the Q and $\overline{Q}$ outputs and should be terminated with higher values of resistance. Typically 4 kΩ connected to the minus supply will be acceptable.

Feedthrough of noise from the data bus can cause jitter on the delayed output of the AD9500. If the AD9500 is in the latched mode and the data bus is switching while a delay is being performed, jitter will be seen on the delayed signal. In applications where this situation occurs, it is recommended that an external latch be used. When using the latch of the AD9500, care must be taken to ensure that the voltage on the data bus does not exceed the $+V_S$ of the device. Data stored in the latch will be lost if this condition exists. The problem is prevalent when the data bus is tristated, or the driving logic has high V_{OH} (HCT), or high slew rate (ACT). In each of these conditions noise or switching can carry the voltage above $+V_S$.

Using an external latch with the device is the best way to alleviate the problem. The AD9501 does not exhibit this condition.

Using the AD9500 with TTL Signals

In applications where maximum update rate is required and TTL compatibility must be maintained, the AD9500 can be configured as shown in Figure 7. The $\overline{TRIGGER}$ pin is biased to a level which is at the switching threshold of a TTL signal. The TRIGGER input is connected to a TTL signal. The RESET and $\overline{RESET}$ inputs cannot tolerate TTL levels and must be resistively divided as shown.

The outputs of the AD9500 cannot drive TTL logic directly. Their swing is approximately 1 V peak-to-peak. These output signals can be offset and the levels made TTL compatible with the addition of the output circuit shown in Figure 7.

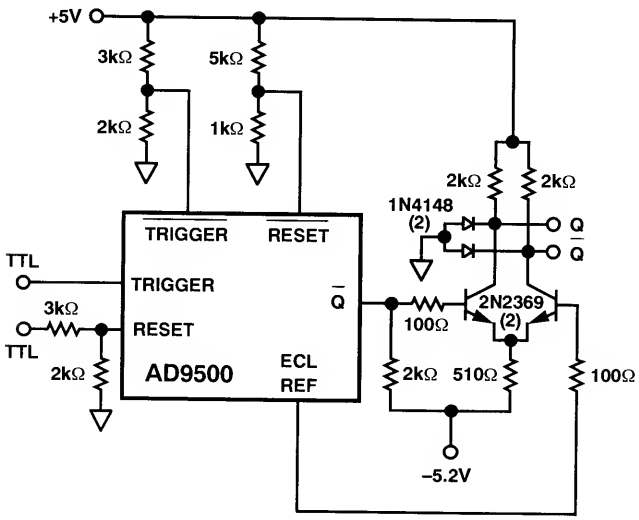


Figure 7. Interfacing the AD9500 with TTL

The smaller prop delay and the faster reset time of the AD9500 can be utilized for faster update rates. If the performance specifications of the AD9501 fit the application, it should be used in lieu of an AD9500 configured in the TTL mode.

Programmable Oscillator with Enable

An AD9501 configured as a programmable oscillator is shown in Figure 8. The frequency of oscillation is controlled by programming the AD9501 delay and can be determined by the equation shown below. The enable input allows the oscillator to be switched on and off, which is a useful feature in many applications.

Freq = 1 / [AD9501 Prop Delay + AD9501 Program Delay + AD9501 Reset Prop Delay + (3 × U1 Prop Delay)]

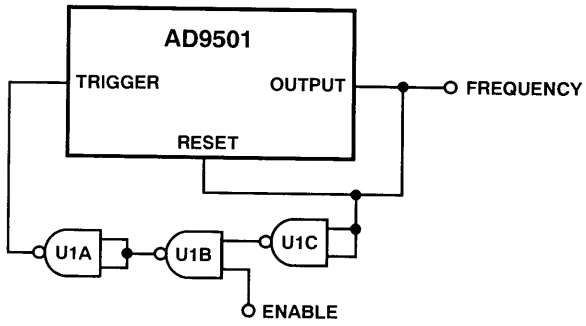


Figure 8. The AD9501 Configured as a Programmable Oscillator

Delaying A Pulse

The AD9500 and AD9501 delay only one edge of the input trigger pulse. The trigger pulse is not replicated at the output of the device. To preserve the pulse width of the input signal, two delay generators must be used as shown in Figure 9. The full-scale range and program delay are set to the same values on both devices. Delay Generator 1 delays the rising edge of the input pulse, while Delay Generator 2 delays the falling edge.

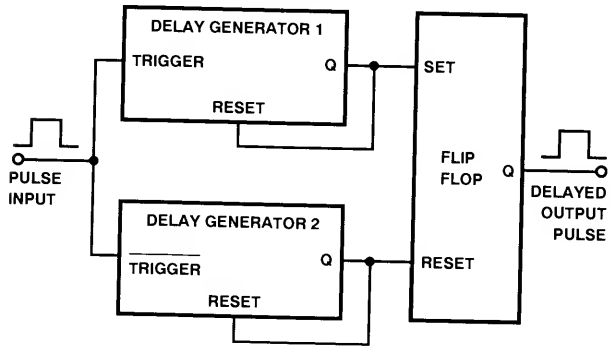


Figure 9. Two Delay Generators Used to Delay Both Input Pulse Edges to Main Pulse Width at the Output

Multichannel Deskewing

High speed systems with parallel signal paths require that close delay matching be maintained. Delay mismatch can cause error in data transfer. Much of this skew can be eliminated by running each signal through a delay generator and adjusting the program delays to minimize the timing skews. With the very fine timing adjustments possible from the AD9500 and AD9501, most high speed systems should be able to adjust automatically to extremely tight tolerances. Figure 10 illustrates a typical deskew application. A method of performing the calibration of multiple delay generators is shown in Figure 11. At the test head, the DUT socket is shorted from input to output. The Q output of the flip flop is monitored for the switching threshold of the delay generator as the digital delay code is varied. Each delay generator is adjusted separately with this offset delay stored in its latch. Calibration is complete when each delay generator is adjusted.

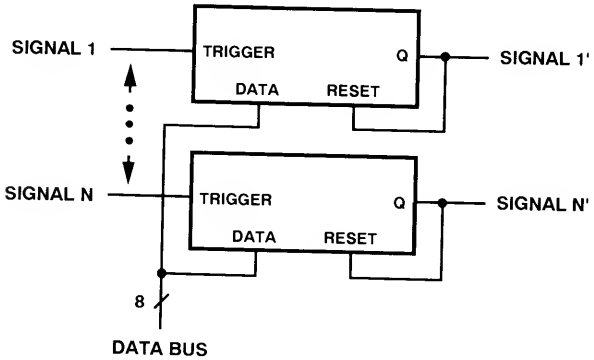


Figure 10. Multiple Signal Deskewing

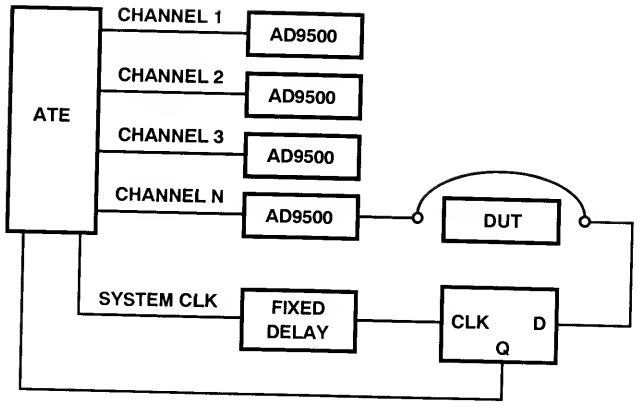


Figure 11. Automatic Calibration for ATE Deskew

Laser Applications

Laser light differs from other light sources in that it is coherent. Laser light is usually monochromatic and highly collimated. Because lasers are stable, emit sharp spectral lines, and are convenient to use, they are found in applications such as range measurement; atmospheric monitoring; industrial cutting, welding, and drilling; laser printers; computer laser disk drives; spectrometry; and communication.

In most of these applications, the laser is a pulsed beam of light which must be synchronized to an external event. The AD9500 and AD9501 provide an easy means for this synchronization, and allow calibration. A programmable delay generator can be used to control the timing and duration of a laser pulse with respect to an external event. In systems with two or more lasers, synchronization can also be controlled with a delay generator.

The duration of laser pulses is usually short, tens of nanoseconds, and the repetition rate is fairly low, tens of kilohertz. Full-scale range must be set small so that jitter induced by the delay generator does not corrupt the required synchronization of the system. This usually means the full-scale range is set to much less than a cycle of the laser pulse repetition rate, typically 100 ns–300 ns. A fixed coarse delay may have to be used in conjunction with a fine tune programmable delay generator to cover the range of interest to provide the required accuracy.

Pulse Width Modulation (PWM)

Another application for the AD9500/AD9501 is pulse width modulation (PWM) in laser printers. PWM allows a laser printer to print gray shades instead of just black and white images.

In normal operation a pulse is supplied to a laser diode driver which turns the laser diode completely on or off. When the diode is on, toner is deposited on the drum, and when the diode is off, no toner is deposited. This image is then transferred to paper. The image will be black and white.

By controlling the laser diode pulse width, varying shades of gray may be generated. Using two AD9501s as shown in Figure 12, the pulse width can be modulated digitally. Digital modulation allows tremendous flexibility and repeatability in creating gray shade images.

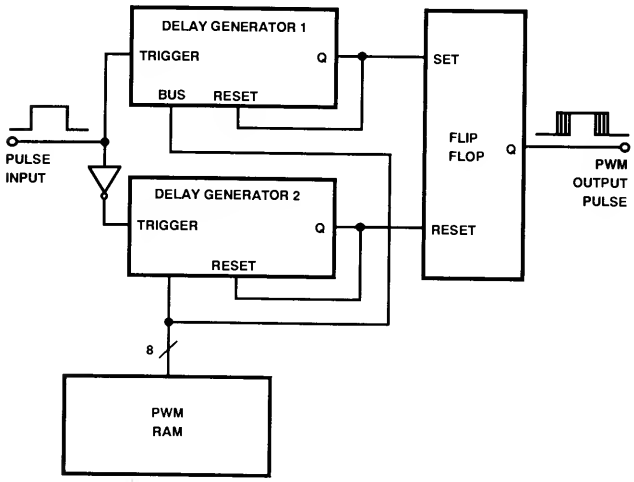


Figure 12. Laser Printer PWM

Layout Considerations

Although the AD9500 and AD9501 are designed to interface with digital signals, they are inherently analog circuits. It is therefore critical to use high speed analog circuit layout techniques. The ground connections to the device should be a low impedance connection to a solid ground plane. The plane should extend under the device to shield it from digital switching signals.

Most socket assemblies add significant interlead capacitance, and should be avoided whenever possible. If sockets must be used, individual pin sockets such as AMP Part Number 6-330808-0 should be used. Prototyping on wirewrap or vector board is strongly discouraged.

Power supply decoupling is also critical for high speed design; a 0.1 μF capacitor should be connected as close as possible to each supply pin.

Even in applications where the devices will be updated at slow rates and the programmed delays will be very long, the above considerations must be taken into account.